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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,489	08/07/2003	Mao-Yi Chang	CHAN3214/EM	1409

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EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,489	CHANG ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-19* is/are pending in the application.

4a) Of the above claim(s) *7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-6, 8, 9 and 11-13, 15-17 and 19 are rejected under 35 U. S. C. 102(e) as being anticipated by Voutsas (US Pat. 6,649,032).

Voutsas discloses a method for transforming an amorphous silicon layer into a polysilicon layer, comprising: providing an amorphous silicon layer (a-Si 306) (fig. 3 and col. 2, lines 40-49), and doping amorphous silicon layer with an inert gas atom (Ar) (See Abstract and col. 4, lines 16-19 & lines 37-39); and heating the surface of amorphous silicon substrate by excimer a laser process. The amorphous layer of Voutsas can be considered to consist of two layers (amorphous silicon buffer layer and amorphous silicon layer) with the same composition (amorphous silicon layer). When a layer of amorphous material is depostied upon a layer of the same material, there is no detectable boundary between these layers. This is due to the fact that amorphous materials do not contain crystal grain boundaries. In other words, when looking at a cross-section of these two layers, one cannot determine where one layer ends and another begins.

An amorphous layer can be deposited as one layer or a stack of multiple thin layers. However, the end product will be the same. In other words, "amorphous silicon buffer layer" and " amorphous silicon layer " are merely broad limitations that encompass amorphous silicon layers.

2. Claims 1-6, 8-10 and 12-18 are rejected under 35 U. S. C. 102(e) as being anticipated by Yamazaki et al. (US Pat. 6,812,081, herein after Yamazaki).

Regarding claims 1 and 12, Yamazaki discloses a method for transforming an amorphous silicon layer into a polysilicon layer, comprising: providing an amorphous silicon layer, and doping amorphous silicon layer with an inert gas atom; and heating the surface of amorphous silicon substrate by heat treatment or thermal process (col. 2, lines 40-51; col. 4, line 66 through col. 5, line 11). The amorphous layer of Yamazaki can be considered to consist of two layers (amorphous silicon buffer layer and amorphous silicon layer) with the same composition (amorphous silicon layer). When a layer of amorphous material is depostied upon a layer of the same material, there is no detectable boundary between these layers. This is due to the fact that amorphous materials do not contain crystal grain boundaries. In other words, when looking at a cross-section of these two layers, one cannot determine where one layer ends and another begins. An amorphous layer can be deposited as one layer or a stack of multiple thin layers. However, the end product will be the same. In other words, "amorphous silicon buffer layer" and " amorphous silicon layer " are merely broad limitations that encompass amorphous silicon layers.

Regarding claims 2 and 15, Yamazaki discloses that inert gas atom is selected from a group consisting of helium, neon, argon, krypton, xenon (col. 7, lines 42-59).

Regarding claims 3 and 17, Yamazaki discloses that inert gas atom is argon (col. 2, lines 1-5 & 42-43).

Regarding claims 4 and 16, Yamazaki discloses the atom percentage of inert gas atom in amorphous silicon layer is 0.006 (in the range of from 1 to 0.001) {Yamazaki discloses in col. 2, lines 45-46 that the concentration of Ar in the amorphous silicon layer is $3x10^{20}/cm^3$; therefore $3x10^{20}/cm^3$ (Ar)/ $5x10^{22}/cm^3$ (Si) = 0.006}.

Regarding claims 5-6, Yamazaki discloses that inert gas atom is doped by plasma chemical vapor deposition (col. 7, lines 60-67 & 22-27).

Regarding claim 8, Yamazaki discloses that polysilicon substrate is a panel of a liquid crystal display (col. 24, lines 8-14).

Regarding claims 9 and 13, Yamazaki discloses that heat treatment is an excimer laser annealing (col. 8, lines 56-59).

Regarding claims 10 and 14, Yamazaki discloses that the process window of excimer laser is in the range of from 100 to 400 mJ/cm^2 (col. 13, line 66 through col. 14, line 1).

Regarding claim 18, Yamazaki discloses that inert gas atom is doped by continuous laser pulses (col. 14, lines 3-6 & Abstract).

Response to Arguments

3. Applicant's arguments filed 12/08/05 have been fully considered but they are not persuasive.

Applicant argues that the inert gas in the prior art (Voutsas) is not for doping an already formed amorphous silicon layer as claimed in the present application. This argument is not

convincing, especially since Voutsas teaches "...The low hydrogen content polycrystalline silicon films are made from introducing a small amount of hydrogen gas, with Ar, during the sputter deposition of an amorphous silicon film...." (see Abstract). Therefore, Voutsas, as indicated in the above rejection, clearly discloses claimed features.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID VU
PRIMARY EXAMINER